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L20	l4 and l6	3	L20
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L15	l1 and l5	4	L15
L14	l10 and l8	22	L14
L13	l10 and l7	45	L13
L12	l10 and l6	3	L12
L11	l10 and l5	25	L11
L10	boolean and short$4 near4 circuit$3 and (conjugat$4 or "OR" or "AND")	1042	L10

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L9	boolean and short$4 near4 circuit$3 and (conjugat$4 or "OR" or "AND")	1023	L9
L8	(326/41;114,125)[CCLS]	1674	L8
L7	(716/16-19)[CCLS]	3368	L7
L6	(712/200-203,223, 225,227,228)[CCLS]	1014	L6
L5	(712/2-300)[CCLS]	12758	L5

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L4	(programmable or programable or interact$5 or dynamic$6) near25 boolean and short$4 near4 circuit$3	73	L4
L3	dynamic$6 near25 boolean and short$4 near4 circuit$3	13	L3
L2	l1 and static$4	18	L2
L1	boolean and short$4 near4 circuit$3 near15 (conjugat$4 or "OR" or "AND")	50	L1

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Kodandapani, K.L.; Pradhan, D.K.;
Computers, IEEE Transactions on
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Bhattacharya, B.B.; Gupta, B.;
Computers, IEEE Transactions on
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☐ **3. Detection of stuck-at and bridging faults in Reed-Muller canonical (RMC) networks**
Damaria, T.; Karpovsky, M.;
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Comte, M.; Ohtake, S.; Fujiwara, H.; Renovell, M.;
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☐ **5. Testing for resistive shorts in FPGA Interconnects**
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Digital Object Identifier 10.1109/ISQED.2005.120

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